查询LCDA15C-6供应商

SEMTECH

LCDA15C-6
Low Capacitance TVS Diode Array For Multi-mode Tranciever Protection

PROTECTION PRODUCTS

Description

The LCDA15C-6 has been specifically designed to protect sensitive components which are connected to data and transmission lines from over voltages caused by **ESD** (electrostatic discharge), **EFT** (electrical fast transients), and **lightning**.

The low capacitance array configuration of the LCDA15C-6 allows the user to protect six high-speed data or I/O lines. They may be used on systems operating from 5 to 15 Volts. The high surge capability (500W, tp=8/20µs) makes the LCDA15C-6 suitable for telecommunications systems operating in harsh transient environments. The low inductance construction minimizes voltage overshoot during high current surges.

The features of the LCDA15C-6 are ideal for protecting multi-protocol transceivers in WAN applications such as Frame Relay systems, routers, and switches.

Features

- Transient protection for high-speed data lines to
  IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 0.5kV, 12A (8/20µs)
- Protects six I/O lines
- Low capacitance for high-speed interfaces
- High surge capability
- Low clamping voltage
- Solid-state silicon avalanche technology

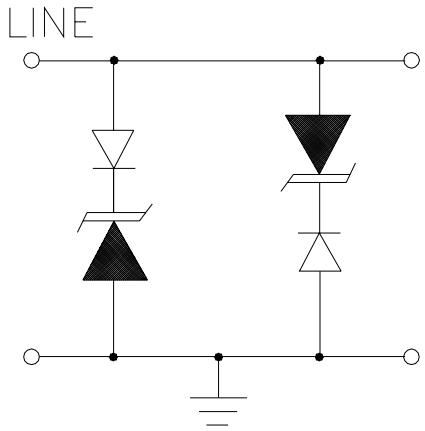
Mechanical Characteristics

- JEDEC SO-8 package
- Molding compound flammability rating: UL 94V-0
- Marking : Part number, date code, logo
- Packaging : Tape and Reel per EIA 481

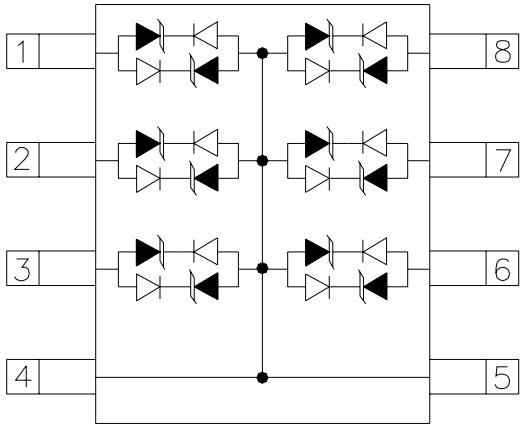
Applications

- Multi-Mode Transceiver Protection
- WAN Equipment:
  - CSU/DSU
  - Multiplexers
  - Routers
  - ISP Equipment
  - Customer Premise Equipment
- Protection for any of the following interfaces:
  - RS-232 (V.28)
  - RS-422 (V.11, X.21)
  - RS-449 (V.11/V.10)
  - RS-485

Circuit Diagram



Schematic & PIN Configuration



SO-8 (Top View)

PROTECTION PRODUCTS

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	500	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	15	A
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

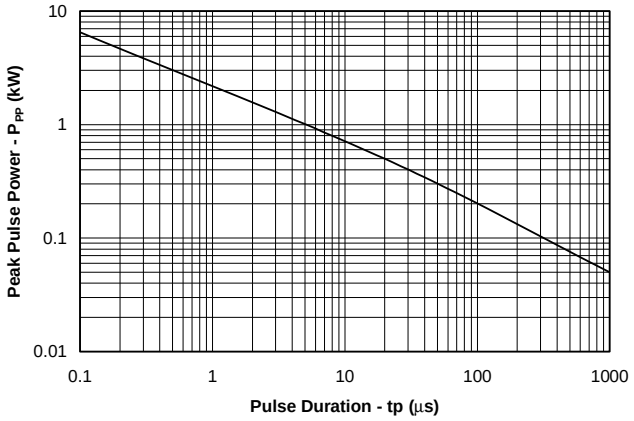
Electrical Characteristics

LCDA15C-6

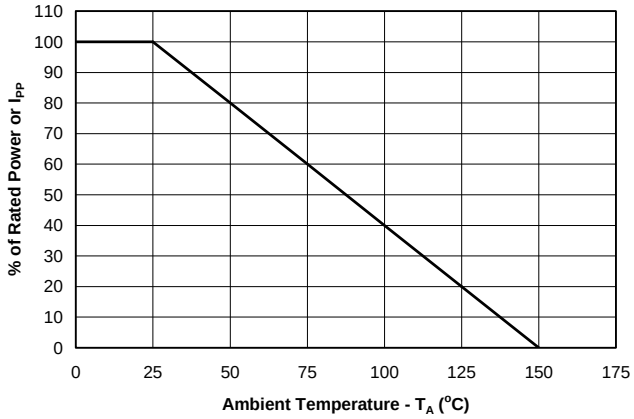
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_t= 1mA	16.7			V
Reverse Leakage Current	I_R	V_{RWM} = 15V, T=25°C			5	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs			24	V
Clamping Voltage	V_C	I_{PP} = 15A, tp = 8/20µs			33	V
Junction Capacitance	C_j	Between I/O pins and Gnd V_R = 0V, f = 1MHz		8	15	pF
		Between I/O pins V_R = 0V, f = 1MHz		3		pF

Typical Characteristics

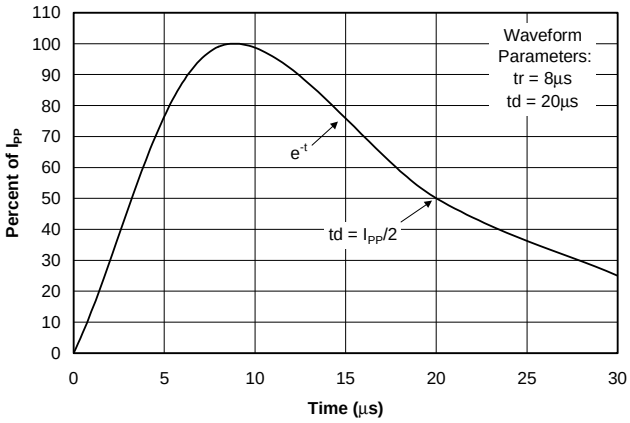
Non-Repetitive Peak Pulse Power vs. Pulse Time



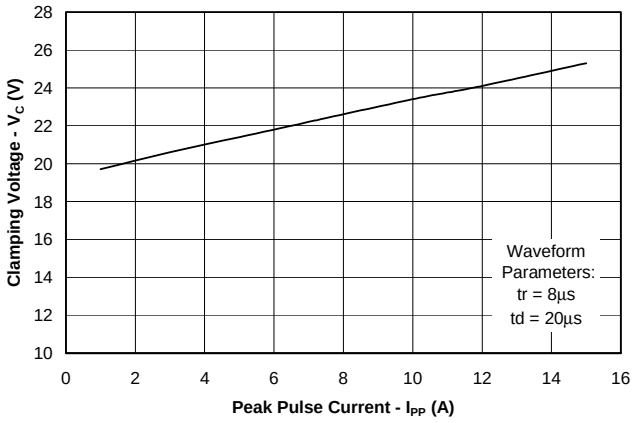
Power Derating Curve



Pulse Waveform



Clamping Voltage vs. Peak Pulse Current

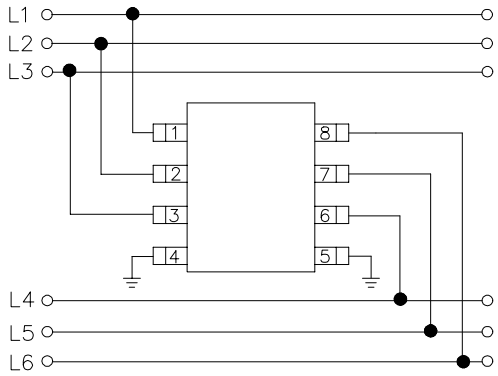


Applications Information

Device Connection Options for Protection of Six High-Speed Data Lines

The LCDA16C-6 may be configured to protect up to six I/O lines operating between 5 and 15V. It may be used to protect the most popular serial data interface standard lines making it ideal for use in equipment utilizing multi-mode transceivers. Data lines are connected at pins 1, 2, 3, 6, 7, and 8. Pins 4 and 5 are connected to ground. For best results, these pins should be connected directly to a ground plane on the board. The path length should be kept as short as possible to minimize parasitic inductance.

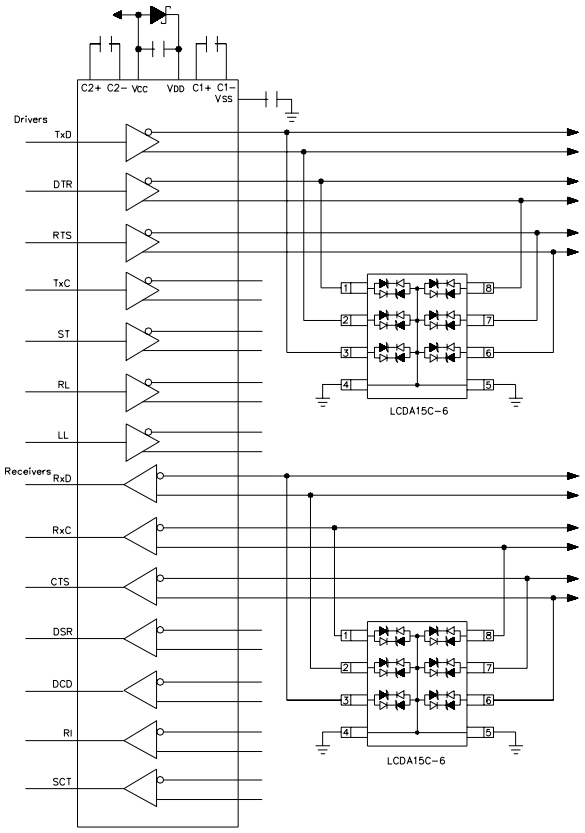
Device Connection



Multi-Mode Transceiver Protection

A typical multi-mode transceiver protection circuit is shown. The LCDA15C-6 is used to protect I/O lines with external connections. The LCDA15C-6 adds a maximum loading capacitance of 15pF with a working voltage of 15V. This allows the transceiver to safely operate in all modes without clipping or degradation of the signal.
With proper design and layout, the transceiver port can be protected to >15kV (HBM per IEC 61000-4-2).

Multi-Mode Tranceiver Protection Example

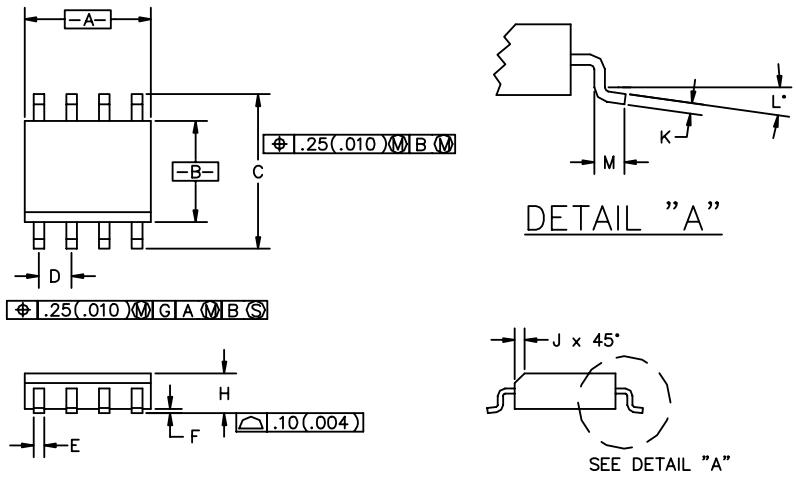


Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended:

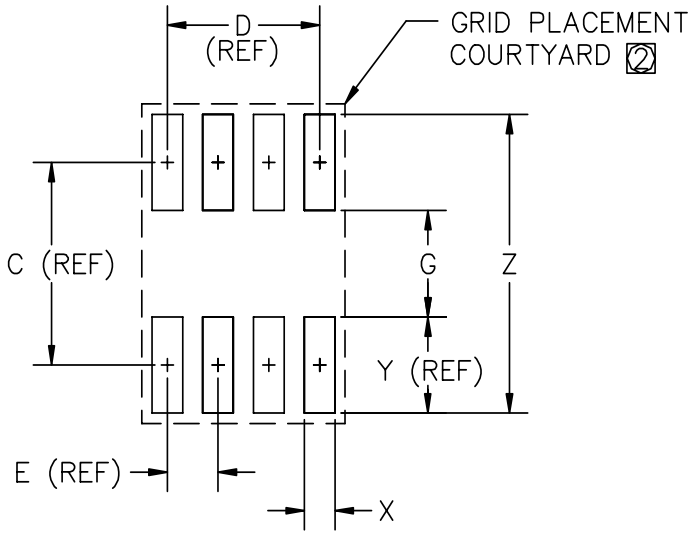
- Place the LCDA15C-6 near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the LCDA15C-6 and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Outline Drawing - SO-8



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

Land Pattern - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

Ordering Information

Part Number	Working Voltage	Qty per Reel	Reel Size
LCDA15C-6.TB	15V	500	7 Inch
LCDA15C-6.TE	15V	2,500	13 Inch

Note:
(1) No suffix indicates tube pack.

Contact Information

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